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Notice of Allowability	Application No.	Applicant(s)	
	09/625,643	HIRAGA, NORIAKI	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/22/04*.

2. ☒ The allowed claim(s) is/are *1 - 3, 6 - 8, 46 - 49*.

3. ☒ The drawings filed on *25 July 2000* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

Examiner acknowledges a submission of the amendment and arguments filed on December 22, 2004. Claims 5, 9 - 11, 15 and 16 are deleted; Claims 1, 2 and 6 - 8 are amended. New Claims 46 – 49 are added. Amendment and arguments have overcome rejections under 103(a).

The following is an examiner's statement of reasons for allowance:

An amended independent Claim 1 recites a semiconductor integrated circuit device including, in part, "first transistor forming an input element, connected to said inter-circuit signal wire, in one of said two internal circuits" and "a plurality of second transistors, for protecting said first transistor, being arranged adjacent to said first transistor in said one of said two internal circuits and including a transistor of an identical structure to said first transistor," wherein gates of said plurality of second transistors are connected only to said power liners of said one of said two internal circuits." The closest reference for the recited part of the Claim is Watt (US 5,623,156), which discloses a first transistor forming an input element connected to the inter-circuit signal wire (element 12 in Fig. 5), and a second transistor (element M0 in Fig. 5) protecting the first transistor and having identical structure to the first transistor. The gate of the second transistor is connected only to the power line (line Vssi in Fig. 5). However, it does not disclose a plurality of the second transistors being arranged adjacent to the first transistor. According to Applicant, a location of protecting transistors

adjacent to the protected one is critical. Additionally, a feature of use of plurality of transistors for protection of a single transistor (which is the most vulnerable element of the circuit since it is connected to the inter-circuit signal wire) is novel.

Allowability resides, at least in part, in the above-described limitations, which has not been disclosed in the Prior Art in a search.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (571) 272-2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
02/23/2005

BRIAN SIRCUS
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